**RAKEN**

Engineering Specification

# LCM ENGINEERING
# SPECIFICATION

| *MODEL | LC420EUH |
|--------|----------|
| SUFFIX | RDA1 |
| Update | Jan.28, 2011 |

(   )    **Preliminary Specification**

( ● )    **Final Specification**

| | Engineering Specification | |
|---|---|---|

# CONTENTS

Engineering Specification

# RECORD OF REVISIONS

| Revision No. | Revision Date | Page | Description |
|---|---|---|---|
| 0.1 | Nov 05, 2010 | - | Final Specification (First Draft) |
| 0.2 | Nov 11, 2010 | 5 | Update LED Input voltage (Forward voltage) |
| 0.3 | Dec 15, 2010 | 6, 8 | Electrical spec  is updated |
| | | 12 | Signal Timing  is updated |
| | | 18 | Optical Spec is updated |
| | | 23, 24 | 2D Drawing is updated. |
| | | 31 | LED Array spec is updated.. |
| | | - | Final Specification |
| 0.4 | Dec 20, 2010 | 25 | Table 13.  ENVIRONMENT TEST CONDITION is updated. |
| 0.5 | Jan.13.2011 | 5 | -Updated the Note: The storage test condition and the operating test condition |
| | | 23.24 | -updated mechanical drawing |
| 0.6 | Jan.28.2011 | 12 | -update T6/T7 (data setup time/date hold time) |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

**RAKEN**

Engineering Specification

# 1. General Description

The LC420EUH is a Color Active Matrix Liquid Crystal Display with an integral Light Emitting Diode (LED) backlight system . The matrix employs a-Si Thin Film Transistor as the active element.
It is a transmissive display type which is operating in the normally black mode. It has a 42.02 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array).
Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arrayed in vertical stripes.
Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot.
Therefore, it can present a palette of more than 16.7M(true) colors.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.
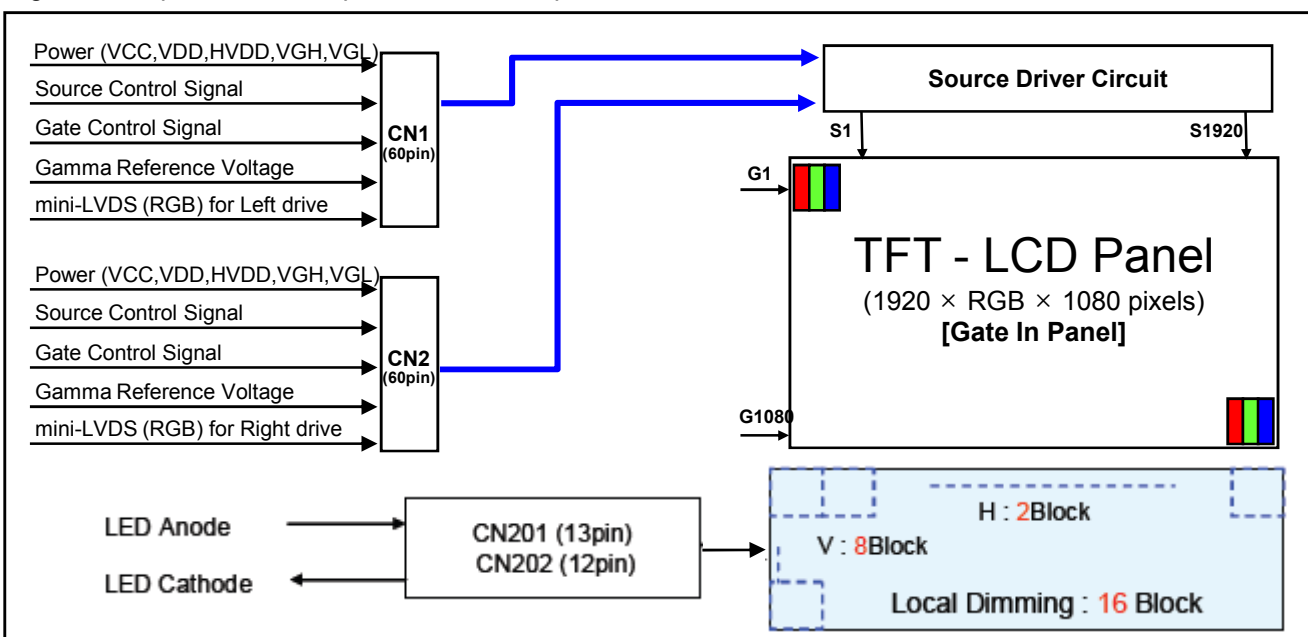


## General Features

| | |
|---|---|
| Active Screen Size | 42.02 inches(1067.31mm) diagonal |
| Outline Dimension | 968.4(H) × 564(V) X 10.8mm(B)**[21.3 mm(User CNT)] (Typ.)** |
| Pixel Pitch | 0.4845 mm x 0.4845 mm |
| Pixel Format | 1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement |
| Color Depth | 8bit,  16,7 M colors (※ 1.06B colors @ 10 bit (D) System Output ) |
| Drive IC Data Interface | Source D-IC : 8-bit mini-LVDS, gamma reference voltage, and control signals<br>Gate D-IC : Gate In Panel |
| Luminance, White | 400 cd/m2 (Center 1point ,Typ.) |
| Viewing Angle (CR>10) | Viewing angle free ( R/L 178 (Min.), U/D 178 (Min.)) |
| Power Consumption | Total 76.6W  [Logic= 8.6W, LED Backlight =.68W] |
| Weight | 7.0 Kg (Typ.) |
| Display Operating Mode | Transmissive mode, normally black |
| Surface Treatment | Hard coating(3H), Anti-glare treatment of the front polarizer (Haze 10%) |

## 2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or permanent damage to the LCD module.

**Table 1.  ABSOLUTE MAXIMUM RATINGS**

| Parameter | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Logic Power Voltage | VCC | -0.5 | +4.0 | V$_{DC}$ | 1 |
| Gate High Voltage | VGH | +18.0 | +30.0 | V$_{DC}$ | |
| Gate Low Voltage | VGL | -8.0 | -4.0 | V$_{DC}$ | |
| Source D-IC Analog Voltage | VDD | -0.3 | +18.0 | V$_{DC}$ | |
| Gamma Ref. Voltage (Upper) | VGMH | ½VDD-0.5 | VDD+0.5 | V$_{DC}$ | |
| Gamma Ref. Voltage (Low) | VGML | -0.3 | ½ VDD+0.5 | V$_{DC}$ | |
| LED Input voltage (Forward voltage) | Vf | - | +58 | V$_{DC}$ | |
| Panel Front Temperature | TSUR | - | +68 | °C | 4 |
| Operating Temperature | TOP | 0 | +50 | °C | 2,3 |
| Storage Temperature | TST | -20 | +60 | °C | |
| Operating Ambient Humidity | HOP | 10 | 90 | %RH | |
| Storage Humidity | HST | 10 | 90 | %RH | |

Note   1. Ambient temperature condition (Ta = 25 ± 2 °C )
2. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be Max 39°C, and no condensation of water.
3. Gravity mura can be guaranteed below 40°C condition.
4. The maximum operating temperatures is based on the test condition that the surface temperature
of display area is less than or equal to 68°C with LCD module alone in a temperature controlled chamber.
Thermal management should be considered in final product design to prevent the surface temperature of
display area from being over 68℃. The range of operating temperature may be degraded in case of
improper thermal management in final product design.
5. The storage test condition:-20℃ temperature/90% humidity to 60℃ temperature/40% humidity ;
the operating test condition: 0℃ temperature/90% humidity to 50℃ temperature/60% humidity.
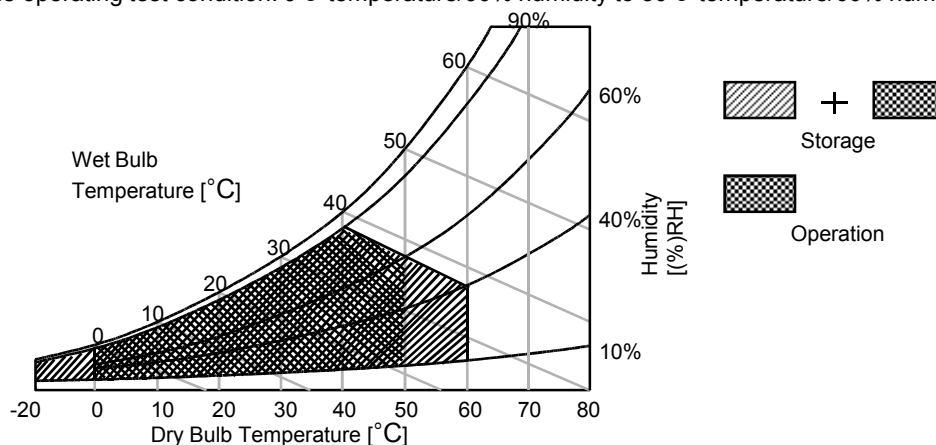
Engineering Specification

## 3. Electrical Specifications

### 3-1. Electrical Characteristics

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and GIP.

**Table 2. DC ELECTRICAL CHARACTERISTICS**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Unit | Note |
|---|---|---|---|---|---|---|---|
| Logic Power Voltage | VCC | - | 3.0 | 3.3 | 3.6 | V$_{DC}$ | |
| Logic High Level Input Voltage | V$_{IH}$ | - | 2.7 | - | VCC | V$_{DC}$ | |
| Logic Low Level Input Voltage | V$_{IL}$ | - | 0 | - | 0.6 | V$_{DC}$ | |
| Source D-IC Analog Voltage | VDD | - | 16.5 | 16.7 | 16.9 | V$_{DC}$ | |
| Half Source D-IC Analog Voltage | H_VDD | - | 8.13 | 8.35 | 8.57 | V$_{DC}$ | 7 |
| Gamma Reference Voltage | V$_{GMH}$ | (GMA1 ~ GMA9) | ½*VDD | - | VDD-0.2 | V$_{DC}$ | |
| | V$_{GML}$ | (GMA10 ~ GMA18) | 0.2 | - | ½*VDD | V$_{DC}$ | |
| Common Voltage | Vcom | Normal | 6.8 | 7.1 | 7.4 | V | |
| | | Reverse | 6.8 | 7.1 | 7.4 | V | |
| Mini-LVDS Clock frequency | CLK | 3.0V≤VCC ≤3.6V | | - | 312 | MHz | |
| mini-LVDS input Voltage (Center) | V$_{IB}$ | Mini-LVDS Clock and Data | 0.7 + (VID/2) | - | (VCC-1.2) − VID / 2 | V | 5 |
| mini-LVDS input Voltage Distortion (Center) | ΔV$_{IB}$ | | - | - | 0.8 | V | |
| mini-LVDS differential Voltage range | V$_{ID}$ | | 200 | - | 800 | mV | |
| mini-LVDS differential Voltage range Dip | ΔV$_{ID}$ | | 25 | - | 800 | mV | |
| Gate High Voltage | VGH | @ 25℃ | 27.7 | 28 | 28.3 | V$_{DC}$ | |
| | | @ 0℃ | 29.6 | 29.8 | 30.0 | V$_{DC}$ | |
| Gate Low Voltage | VGL | - | -5.2 | -5.0 | -4.8 | V$_{DC}$ | |
| GIP Bi-Scan Voltage | VGI_P VGI_N | - | VGL | - | VGH | V$_{DC}$ | |
| GIP Refresh Voltage | VGH even/odd | - | VGL | - | VGH | V | |
| GIP Start Pulse Voltage | VST | - | VGL | - | VGH | V | |
| GIP Operating Clock | GCLK | - | VGL | - | VGH | V | |
| Total Power Current | I$_{LCD}$ | - | | 715 | 929 | mA | 1 |
| Total Power Consumption | PL$_{CD}$ | - | | 8.6 | 11.54 | Watt | 1 |

Note: 1. The specified current and power consumption are under the V$_{LCD}$=12V., 25 ± 2°C, f$_V$=120Hz ondition whereas mosaic pattern(8 x 6) is displayed and f$_V$ is the frame frequency.(with LGD T-Con board)
2. The above spec is based on the basic model.
3. All of the typical gate voltage should be controlled within 1% voltage level
4. Ripple voltage level is recommended under 10%
5. In case of mini-LVDS signal spec, refer to Fig 2 for the more detail.
6. Logic Level Input Signal : SOE,POL,GSP,H_CONV,OPT_N
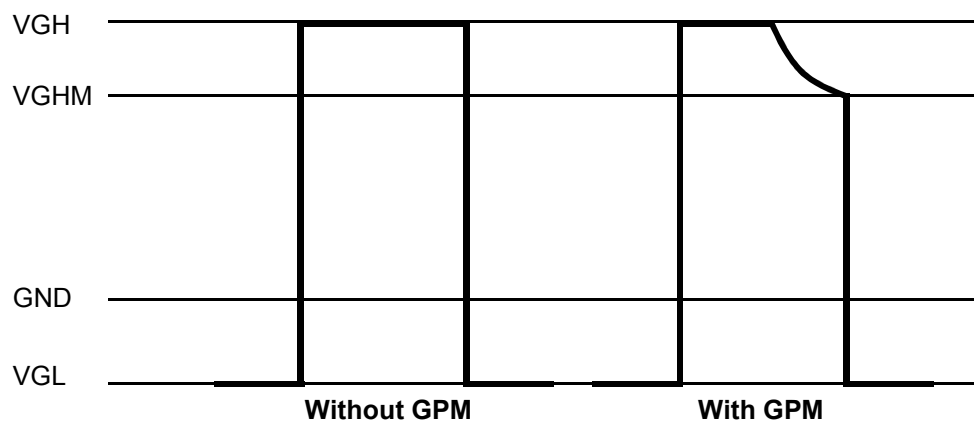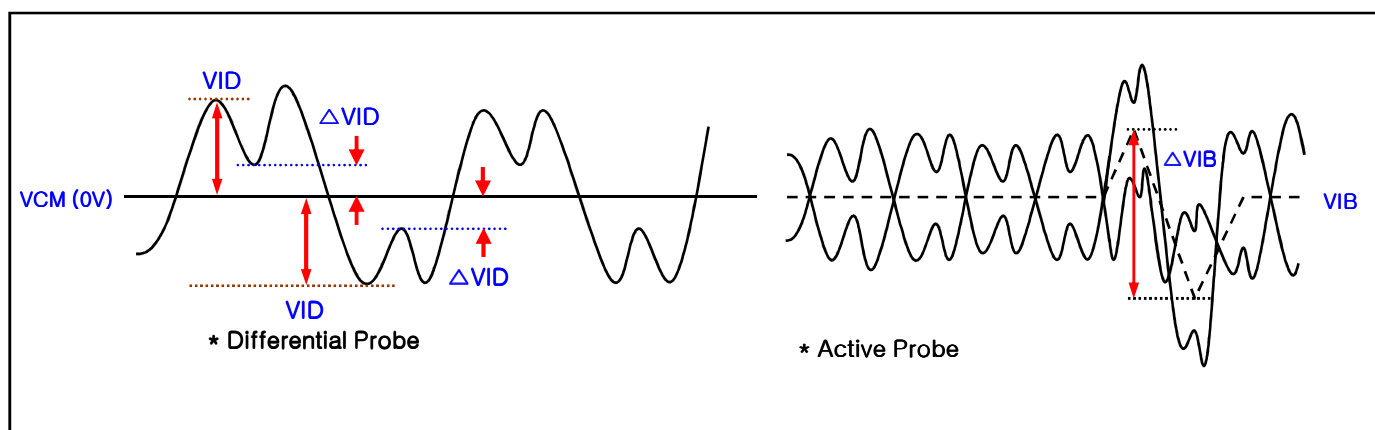7. HVDD Voltage level is half of VDD and it should be between Gamma9 and Gamma10.

**FIG. 1 Gate Output Wave form without GPM and with GPM**
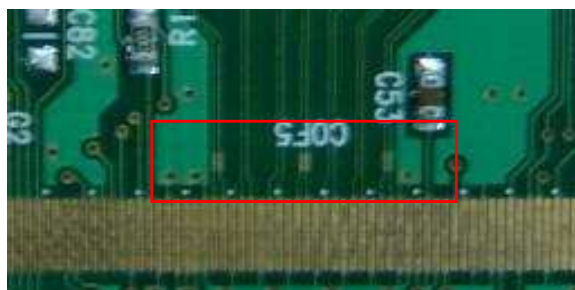


**FIG. 2 Description of VID, ΔVIB, ΔVID**

⋆ Source PCB



**FIG. 3 Measure point**

Engineering Specification

## Table 3. ELECTRICAL CHARACTERISTICS (Continue)

| Parameter | | Symbol | Values | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Backlight Assembly :** | | | | | | | |
| Forward Current (one array) | Anode | $I_{F (anode)}$ | | 380 | | mAdc | ±5% |
| | Cathode | $I_{F (cathode)}$ | 90.25 | 95 | 99.75 | mAdc | 2, 3 |
| Forward Voltage | | $V_F$ | 40.6 | 44.8 | 49 | Vdc | 4 |
| Forward Voltage Variation | | $\triangle V_F$ | | | 1.7 | Vdc | 5 |
| Power Consumption | | $P_{BL}$ | 61.2 | 68 | 74.5 | W | 6 |
| Burst Dimming Duty | | On duty | 1 | | 100 | % | |
| Burst Dimming Frequency | | 1/T | 95 | | 182 | Hz | 8 |
| **LED Array : (APPENDIX-III)** | | | | | | | |
| Life Time | | | 30,000 | 50,000 | | Hrs | 7 |

Notes : The design of the LED driver must have specifications for the LED array in LCD Assembly.
The electrical characteristics of LED driver are based on Constant Current driving type.
The performance of the LED in LCM, for example life time or brightness, is extremely influenced by the characteristics of the LED Driver. So, all the parameters of an LED driver should be carefully designed. When you design or order the LED driver, please make sure unwanted lighting caused by the mismatch of the LED and the driver (no lighting, flicker, etc) has never been occurred. When you confirm it, the LCD–Assembly should be operated in the same condition as installed in your instrument.

1. Electrical characteristics are based on LED Array specification.
2. Specified values are defined for a Backlight Assembly. (IBL : 2 LED array)
3. Each LED array has 2 anode terminal and 8 cathode terminals.
   The forward current($I_F$) of the anode terminal is 380mA and it supplies 95mA into four strings, respectively
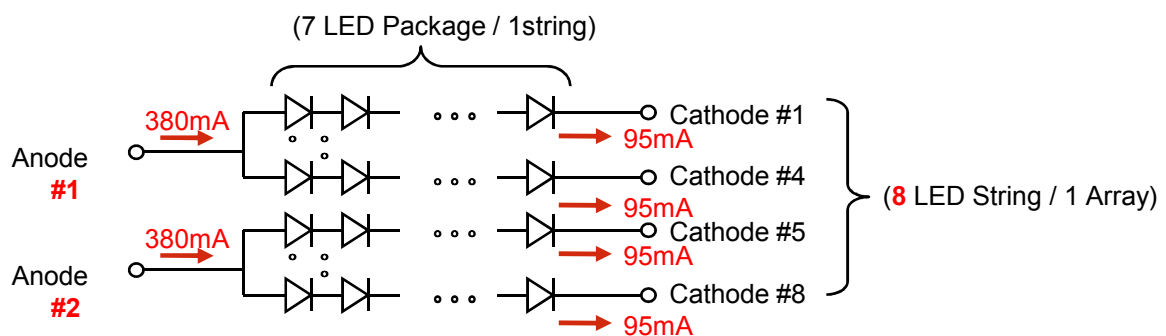


4. The forward voltage($V_F$) of LED array depends on ambient temperature. (Appendix-III)
5. $\Delta V_F$ means Max $V_F$-Min $V_F$ in one Backlight. So $V_F$ variation in a Backlight isn't over Max. 1.7V
6. Maximum level of power consumption is measured at initial turn on.
   Typical level of power consumption is measured after 1hrs aging at 25 ± 2°C.
7. The life time(MTTF) is determined as the time at which brightness of the LED is 50% compared to that of initial value at the typical LED current on condition of continuous operating at 25 ± 2°C, based on duty 100%.
8. The reference method of burst dimming duty ratio.
   It is recommended to use synchronous V-sync frequency to prevent waterfall.(Vsync x 1 =Burst Frequency)
   Though PWM frequency is over 120Hz (max 252Hz), function of LED Driver is not affected.

## 3-2. Interface Connections

This LCD module employs two kinds of interface connection, two 60-pin FFC connector are used for the module electronics and 12-pin,13-pin connectors are used for the integral backlight system.

### 3-2-1. LCD Module

-LCD Connector (CN1): TF06L-60S-0.5SF (Manufactured by HRS)

### Table 4. MODULE CONNECTOR(CN1) PIN CONFIGURATION

| No | Symbol | Description | No | Symbol | Description |
|----|--------|-------------|----|--------|-------------|
| 1 | LTD_OUT | LTD OUTPUT | 31 | LLV4 + | Left Mini LVDS Receiver Signal(4+) |
| 2 | NC | No Connection | 32 | LLV3 - | Left Mini LVDS Receiver Signal(3-) |
| 3 | GCLK1 | GIP GATE Clock 1 | 33 | LLV3 + | Left Mini LVDS Receiver Signal(3+) |
| 4 | GCLK2 | GIP GATE Clock 2 | 34 | LCLK - | Left Mini LVDS Receiver Clock Signal(-) |
| 5 | GCLK3 | GIP GATE Clock 3 | 35 | LCLK + | Left Mini LVDS Receiver Clock Signal(+) |
| 6 | GCLK4 | GIP GATE Clock 4 | 36 | LLV2 - | Left Mini LVDS Receiver Signal(2-) |
| 7 | GCLK5 | GIP GATE Clock 5 | 37 | LLV2 + | Left Mini LVDS Receiver Signal(2+) |
| 8 | GCLK6 | GIP GATE Clock 6 | 38 | LLV1 - | Left Mini LVDS Receiver Signal(1-) |
| 9 | VGI_N | GIP Bi-Scan (Normal =VGL Rotate = VGH) | 39 | LLV1 + | Left Mini LVDS Receiver Signal(1+) |
| 10 | VGI_P | GIP Bi-Scan (Normal =VGH Rotate = VGL) | 40 | LLV0 - | Left Mini LVDS Receiver Signal(0-) |
| 11 | VGH_ODD | GIP Panel VDD for Odd GATE TFT | 41 | LLV0 + | Left Mini LVDS Receiver Signal(0+) |
| 12 | VGH_EVEN | GIP Panel VDD for Even GATE TFT | 42 | GND | Ground |
| 13 | VGL | GATE Low Voltage | 43 | SOE | Source Output Enable SIGNAL |
| 14 | VST | VERTICAL START PULSE | 44 | POL | Polarity Control Signal |
| 15 | GIP_Reset | GIP Reset | 45 | GSP | GATE Start Pulse |
| 16 | VCOM_L_FB | VCOM Left Feed-Back Output | 46 | H_CONV | "H" H 2dot Inversion/ "L" H 1dot Inversion |
| 17 | VCOM_L | VCOM Left Input | 47 | OPT_N | "H" Normal Display / "L" Rotation Display |
| 18 | GND | Ground | 48 | GND | Ground |
| 19 | GND | Ground | 49 | GMA 18 | GAMMA VOLTAGE 18 (Output From LCD) |
| 20 | VDD | Driver Power Supply Voltage | 50 | GMA 16 | GAMMA VOLTAGE 16 |
| 21 | VDD | Driver Power Supply Voltage | 51 | GMA 15 | GAMMA VOLTAGE 15 |
| 22 | H_VDD | Half Driver Power Supply Voltage | 52 | GMA 14 | GAMMA VOLTAGE 14 |
| 23 | H_VDD | Half Driver Power Supply Voltage | 53 | GMA 12 | GAMMA VOLTAGE 12 |
| 24 | GND | Ground | 54 | GMA 10 | GAMMA VOLTAGE 10 (Output From LCD) |
| 25 | VCC | Logic Power Supply Voltage | 55 | GMA 9 | GAMMA VOLTAGE 9 (Output From LCD) |
| 26 | VCC | Logic Power Supply Voltage | 56 | GMA 7 | GAMMA VOLTAGE 7 |
| 27 | GND | Ground | 57 | GMA 5 | GAMMA VOLTAGE 5 |
| 28 | LLV5 - | Left Mini LVDS Receiver Signal(5-) | 58 | GMA 4 | GAMMA VOLTAGE 4 |
| 29 | LLV5 + | Left Mini LVDS Receiver Signal(5+) | 59 | GMA 3 | GAMMA VOLTAGE 3 |
| 30 | LLV4 - | Left Mini LVDS Receiver Signal(4-) | 60 | GMA 1 | GAMMA VOLTAGE 1(Output From LCD) |

Note : 1. Please refer to application note for details.
     (**GIP** & **Half VDD & Gamma Voltage & H_CONV setting**)
2. These 'input signal' (OPT_N,H_CONV) should be connected

-LCD Connector (CN2): TF06L-60S-0.5SF(Manufactured by HRS)

### Table 5. MODULE CONNECTOR(CN2) PIN CONFIGURATION

| No | Symbol | Description | No | Symbol | Description |
|---|---|---|---|---|---|
| 1 | GMA 1 | GAMMA VOLTAGE 1 (Output From LCD) | 31 | RLV1 + | Right Mini LVDS Receiver Signal(1+) |
| 2 | GMA 3 | GAMMA VOLTAGE 3 | 32 | RLV0 - | Right Mini LVDS Receiver Signal(0-) |
| 3 | GMA 4 | GAMMA VOLTAGE 4 | 33 | RLV0 + | Right Mini LVDS Receiver Signal(0+) |
| 4 | GMA 5 | GAMMA VOLTAGE 5 | 34 | GND | Ground |
| 5 | GMA 7 | GAMMA VOLTAGE 7 | 35 | VCC | Logic Power Supply Voltage |
| 6 | GMA 9 | GAMMA VOLTAGE 9 (Output From LCD) | 36 | VCC | Logic Power Supply Voltage |
| 7 | GMA 10 | GAMMA VOLTAGE 10 (Output From LCD) | 37 | GND | Ground |
| 8 | GMA 12 | GAMMA VOLTAGE 12 | 38 | H_VDD | Half Driver Power Supply Voltage |
| 9 | GMA 14 | GAMMA VOLTAGE 14 | 39 | H_VDD | Half Driver Power Supply Voltage |
| 10 | GMA 15 | GAMMA VOLTAGE 15 | 40 | VDD | Driver Power Supply Voltage |
| 11 | GMA 16 | GAMMA VOLTAGE 16 | 41 | VDD | Driver Power Supply Voltage |
| 12 | GMA 18 | GAMMA VOLTAGE 18 (Output From LCD) | 42 | GND | Ground |
| 13 | GND | Ground | 43 | GND | Ground |
| 14 | OPT_N | "H" Normal Display / "L" Rotation Display | 44 | VCOM_R | VCOM Right Input |
| 15 | H_CONV | "H" H 2dot Inversion/ "L" H 1dot Inversion | 45 | VCOM_R_FB | VCOM Right Feed-Back Output |
| 16 | GSP | GATE Start Pulse | 46 | GIP_Reset | GIP Reset |
| 17 | POL | Polarity Control Signal | 47 | VST | VERTICAL START PULSE |
| 18 | SOE | Source Output Enable SIGNAL | 48 | VGL | GATE Low Voltage |
| 19 | GND | Ground | 49 | VGH_EVEN | GIP Panel VDD for Even GATE TFT |
| 20 | RLV5 - | Right Mini LVDS Receiver Signal(5-) | 50 | VGH_ODD | GIP Panel VDD for Odd GATE TFT |
| 21 | RLV5 + | Right Mini LVDS Receiver Signal(5+) | 51 | VGI_P | GIP Bi-Scan (Normal =VGH Rotate = VGL) |
| 22 | RLV4 - | Right Mini LVDS Receiver Signal(4-) | 52 | VGI_N | GIP Bi-Scan (Normal =VGL Rotate = VGH) |
| 23 | RLV4 + | Right Mini LVDS Receiver Signal(4+) | 53 | GCLK6 | GIP GATE Clock 6 |
| 24 | RLV3 - | Right Mini LVDS Receiver Signal(3-) | 54 | GCLK5 | GIP GATE Clock 5 |
| 25 | RLV3 + | Right Mini LVDS Receiver Signal(3+) | 55 | GCLK4 | GIP GATE Clock 4 |
| 26 | RCLK - | Right Mini LVDS Receiver Clock Signal(-) | 56 | GCLK3 | GIP GATE Clock 3 |
| 27 | RCLK + | Right Mini LVDS Receiver Clock Signal(+) | 57 | GCLK2 | GIP GATE Clock 2 |
| 28 | RLV2 - | Right Mini LVDS Receiver Signal(2-) | 58 | GCLK1 | GIP GATE Clock 1 |
| 29 | RLV2 + | Right Mini LVDS Receiver Signal(2+) | 59 | NC | No Connection |
| 30 | RLV1 - | Right Mini LVDS Receiver Signal(1-) | 60 | LTD_OUT | LTD OUTPUT |

Note :  1. Please refer to application note for details
    (**GIP** & **Half VDD & Gamma Voltage & H_CONV setting**)
    2. These 'input signal' (OPT_N,H_CONV) should be connected

**RAKEN**

| Engineering Specification |
|---|

### 3-2-2. Backlight Module

## [ CN201 ]

1) LED Array assy Connector (Plug)

  : 20022HS-13B2(BK) (manufactured by Yeonho)

2) Mating Connector (Receptacle)

  : 20022WR-13BD (manufactured by Yeonho)

## [ CN202 ]

1) LED Array assy Connector (Plug)

  : 20022HS-12B2 (manufactured by Yeonho)

2) Mating Connector (Receptacle)

  : 20022WR-12BD (manufactured by Yeonho )

### Table 6.  BACKLIGHT CONNECTOR PIN CONFIGURATION

| No | Symbol | Description | Note |
|---|---|---|---|
| 1 | Anode_L1 (1~4Cathode) | LED Input Current | |
| 2 | N.C | Open | |
| 3 | L1 Cathode | LED Output Current | |
| 4 | L2 Cathode | LED Output Current | |
| 5 | L3 Cathode | LED Output Current | |
| 6 | L4 Cathode | LED Output Current | |
| 7 | N.C | Open | |
| 8 | L5 Cathode | LED Output Current | |
| 9 | L6 Cathode | LED Output Current | |
| 10 | L7 Cathode | LED Output Current | |
| 11 | L8 Cathode | LED Output Current | |
| 12 | N.C | Open | |
| 13 | Anode_L2 (5~8Cathode) | LED Input Current | |

| No | Symbol | Description | Note |
|---|---|---|---|
| 1 | Anode_R2 (5~8Cathode) | LED Input Current | |
| 2 | N.C | Open | |
| 3 | R8Cathode | LED Output Current | |
| 4 | R7 Cathode | LED Output Current | |
| 5 | R6 Cathode | LED Output Current | |
| 6 | R5 Cathode | LED Output Current | |
| 7 | R4 Cathode | LED Output Current | |
| 8 | R3 Cathode | LED Output Current | |
| 9 | R2 Cathode | LED Output Current | |
| 10 | R1 Cathode | LED Output Current | |
| 11 | N.C | Open | |
| 12 | Anode_R1 (1~4Cathode) | LED Input Current | |

◆ Rear view of LCM
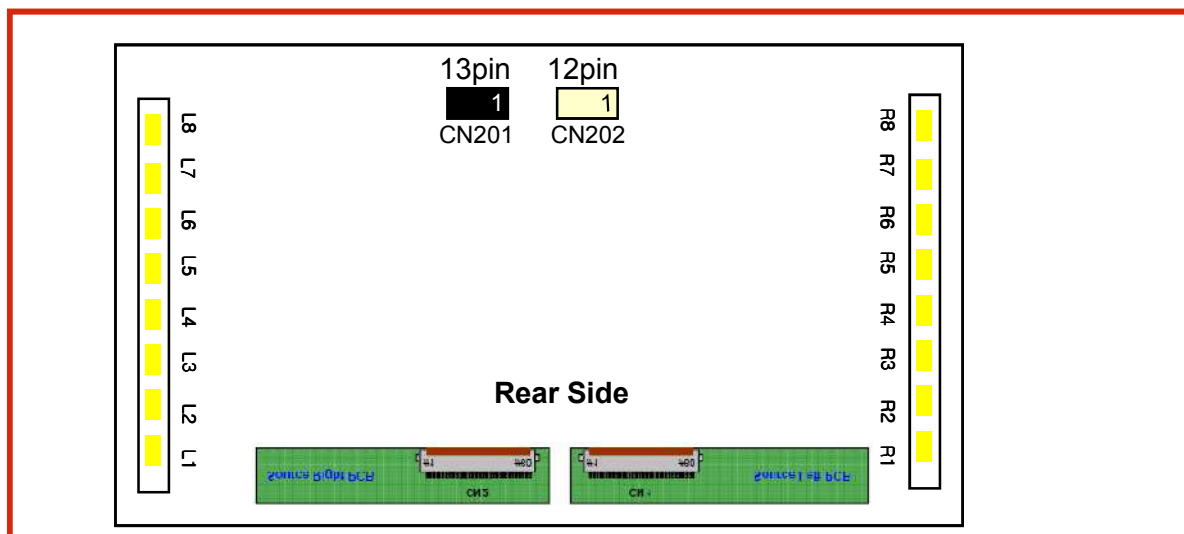
## 3-3. Signal Timing Specification

### TABLE 7. Timing Requirements

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Mini Clock pulse period | T1 | - | 3.2 | 3.4 | | ns | |
| Mini Clock pulse low period | T2 | - | 1.6 | - | - | ns | |
| Mini Clock pulse high period | T3 | - | 1.6 | - | - | ns | 1 |
| Mini Data setup time | T6 | - | 1.1 | - | - | ns | |
| Mini Data hold time | T7 | - | 1.1 | - | - | ns | |
| Reset low to SOE rising time | T8 | - | 0 | - | - | ns | |
| SOE to Reset input time | T9 | - | 200 | - | - | ns | |
| Receiver off to SOE timing | T10 | - | 10 | - | - | CLK cycle | |
| POL signal to SOE setup time | T11 | - | -5 | - | - | ns | |
| POL signal to SOE hold time | T12 | - | 6 | - | - | ns | |
| Reset High Period | T13 | - | Over 50ns & more over 3 CLK | | | CLK cycle | |
| SOE signal GSP setup time | T14 | - | 100 | - | - | ns | |
| SOE signal GSP Hold time | T15 | - | 100 | - | - | ns | |
| SOE signal Pulse Width | T16 | - | 200 | - | - | ns | |

Note :   1. Mini-LVDS timing measure conditions

: 268MHz < Clock Frequency < 312MHz , 200mV < VID < 800mV   @ 3.0<VCC<3.3

2. Setup time and hold time couldn't be satisfied at the same time
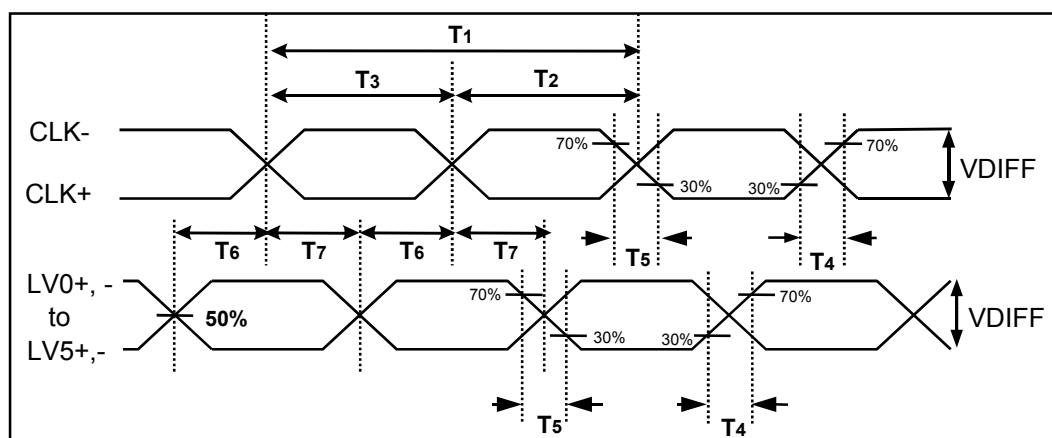


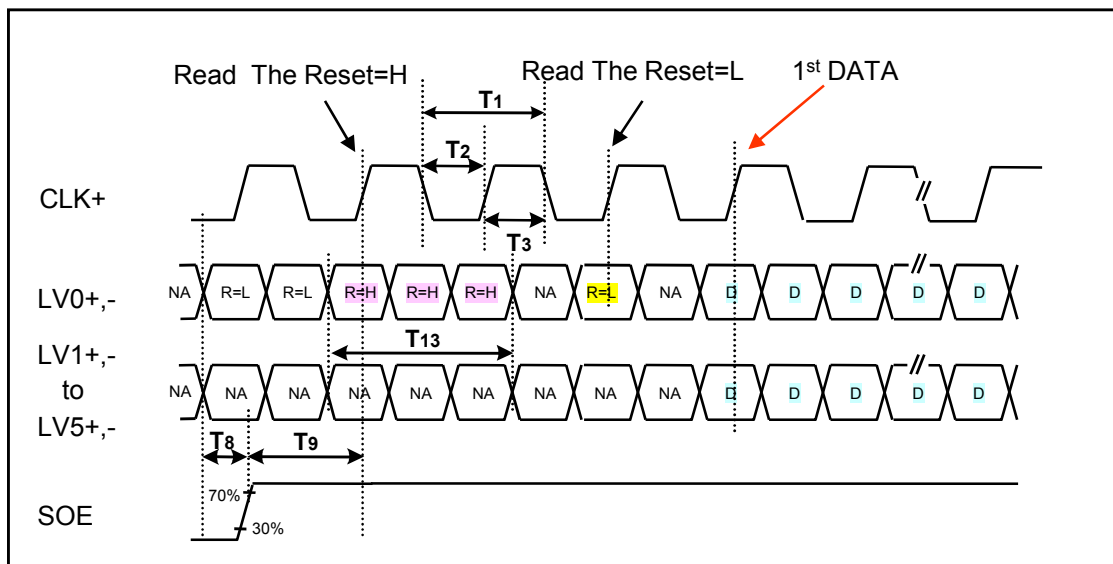**FIG 4. Source D-IC Input Data Latch Timing Waveform**
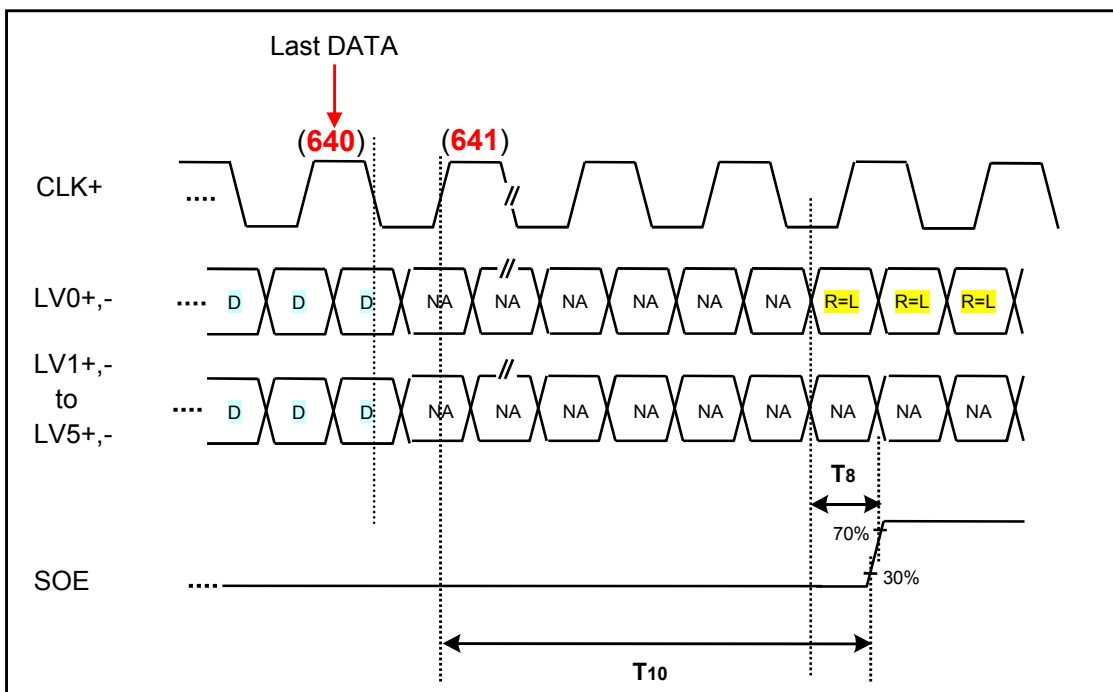
**FIG 5-1. Input Data Timing for 1st Source D-IC Chip**
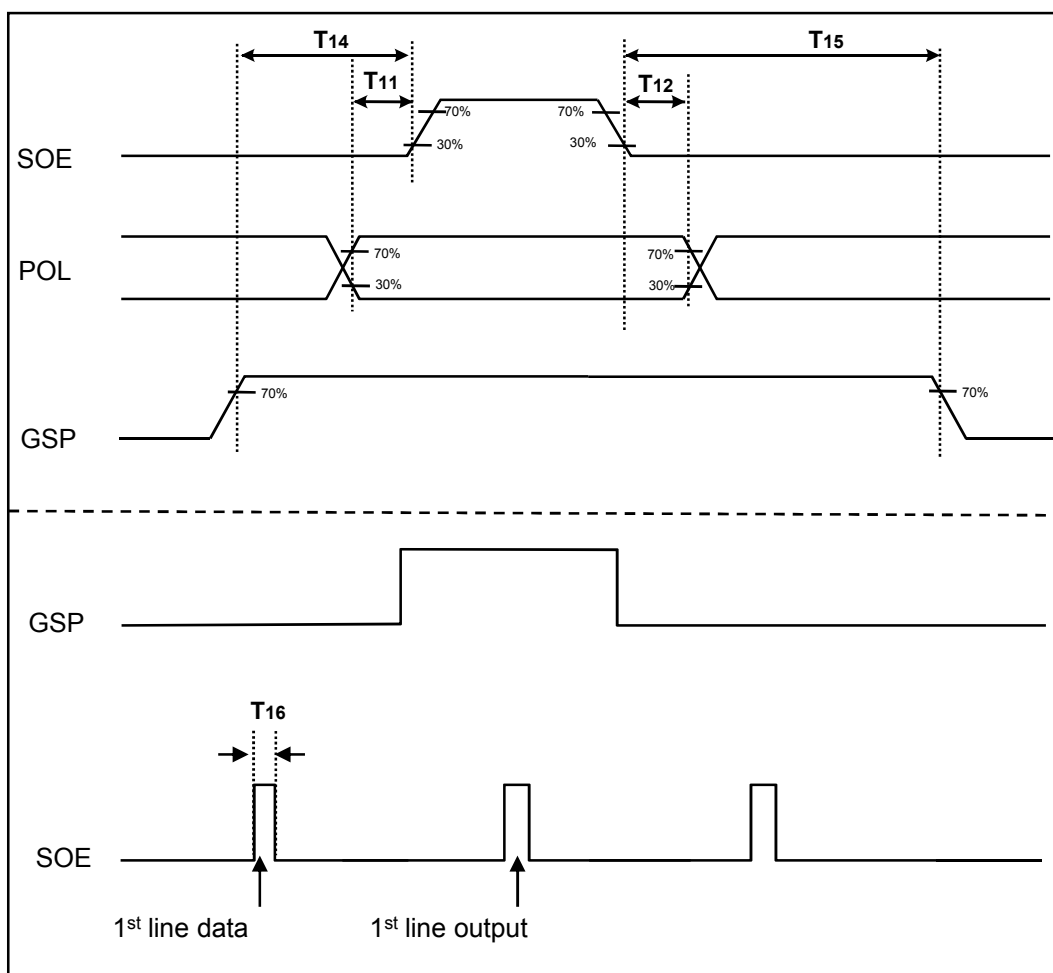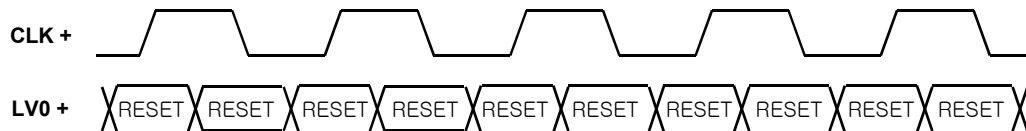


**FIG 5-2. Last Data Latch to SOE Timing**
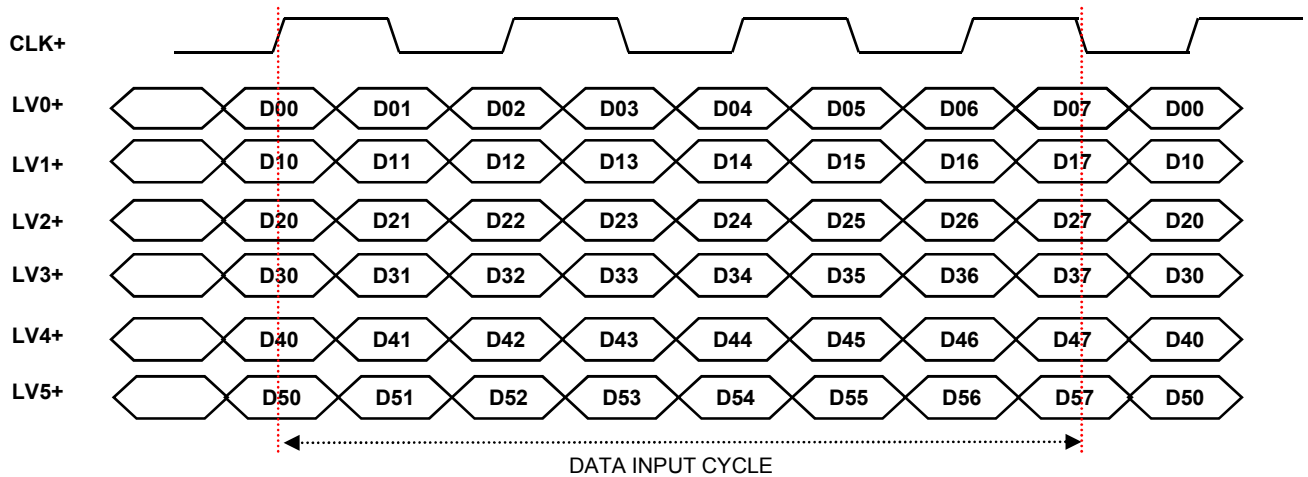
**FIG 6. POL, GSP and SOE Timing Waveform**

## 3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to LV0 to LV5.

### 3-4-1. Control signal input mode

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| CLK + | ‾\_/‾ | \_/‾ | \_/‾ | \_/‾ | \_/‾ | \_/‾ | | | | |
| LV0 + | RESET | RESET | RESET | RESET | RESET | RESET | RESET | RESET | RESET | RESET |

### 3-4-2. Display data input mode

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| LV0+ | | D00 | D01 | D02 | D03 | D04 | D05 | D06 | D07 | D00 |
| LV1+ | | D10 | D11 | D12 | D13 | D14 | D15 | D16 | D17 | D10 |
| LV2+ | | D20 | D21 | D22 | D23 | D24 | D25 | D26 | D27 | D20 |
| LV3+ | | D30 | D31 | D32 | D33 | D34 | D35 | D36 | D37 | D30 |
| LV4+ | | D40 | D41 | D42 | D43 | D44 | D45 | D46 | D47 | D40 |
| LV5+ | | D50 | D51 | D52 | D53 | D54 | D55 | D56 | D57 | D50 |

DATA INPUT CYCLE

**Fig. 7 Mini-LVDS Data**

Note :    1. For data mapping, please refer to panel pixel structure Fig.8
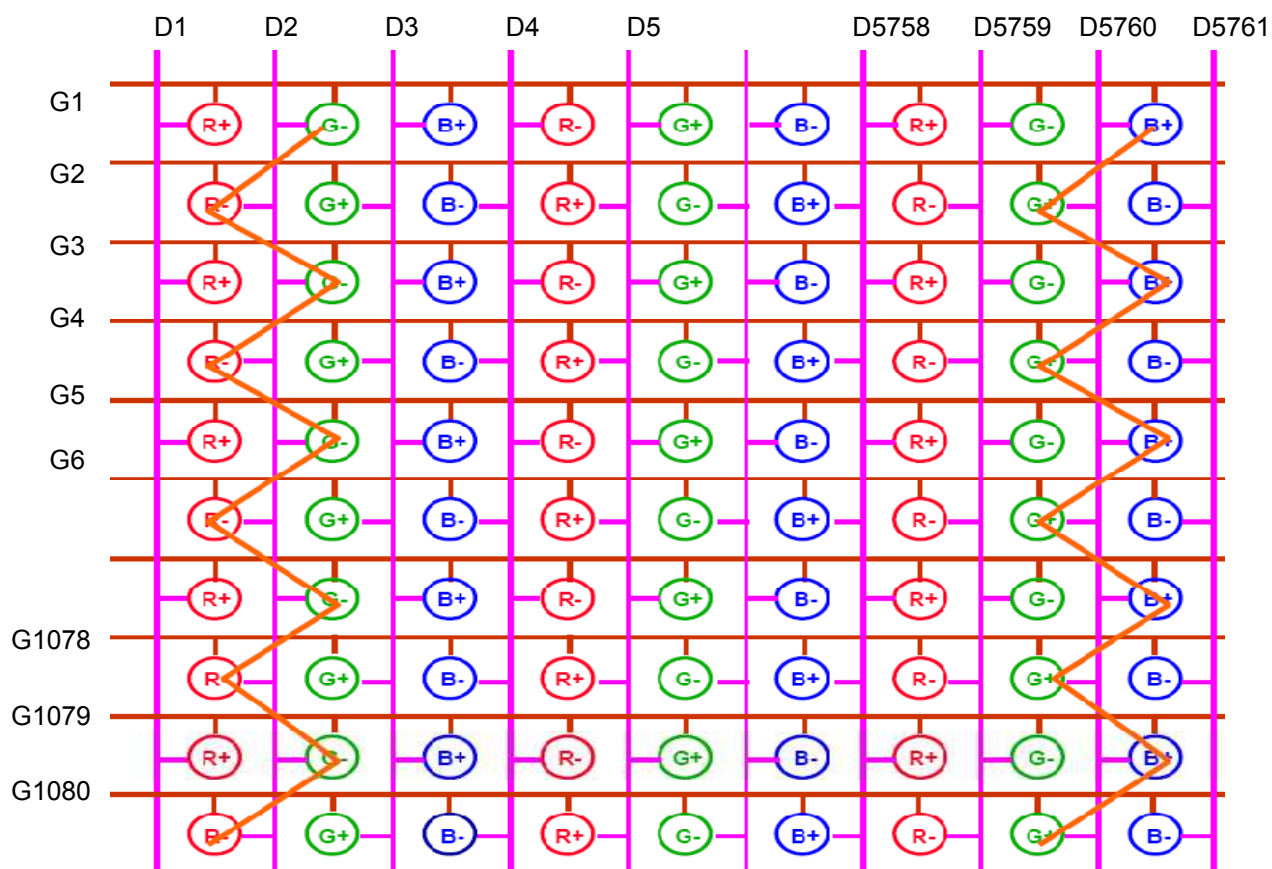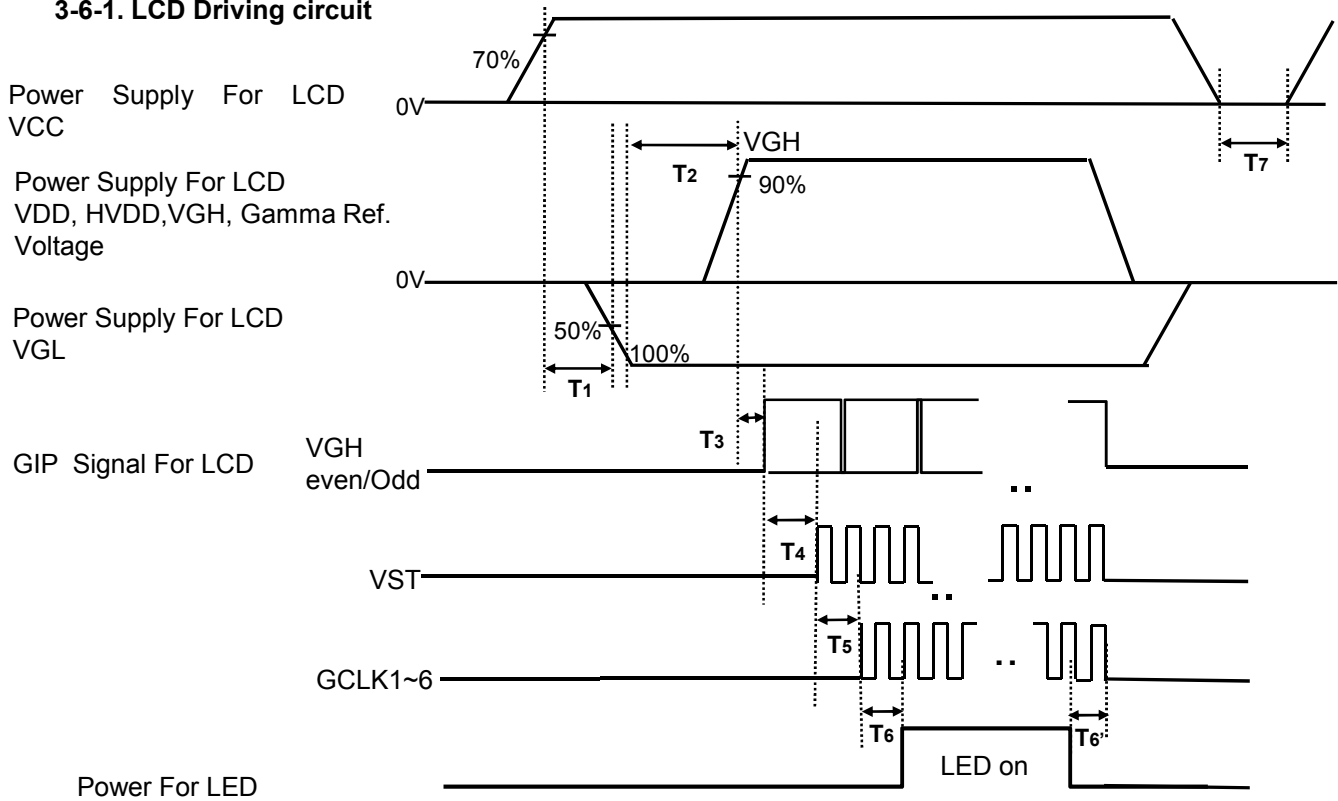
## 3-5. Panel Pixel Structure



**FIG. 8 Panel Pixel Structure**

## 3-6. Power Sequence

### 3-6-1. LCD Driving circuit

Power Supply For LCD VCC

Power Supply For LCD VDD, HVDD,VGH, Gamma Ref. Voltage

Power Supply For LCD VGL

GIP Signal For LCD

Power For LED



### Table 9. POWER SEQUENCE

Ta= 25±2°C, fv=120Hz, Clk=297MHz

| Parameter | Value | | | Unit | Notes |
|-----------|-------|-----|-----|------|-------|
| | Min | Typ | Max | | |
| T1 | 0.5 | | - | ms | |
| T2 | 0.5 | | - | ms | |
| T3 | 0 | | - | ms | |
| T4 | 10 | | - | ms | 2 |
| T5 | 0 | | - | ms | |
| T6 / T6' | 20 | | - | ms | |
| T7 | 2 | | - | sec | |

Note :   1. Power sequence for Source D-IC must follow the Case1 & 2.
          ※ Please refer to Appendix II for more details.
        2. VGH Odd signal should be started "High" status and VGH even & odd can not be "High at the same time.
        3. Power Off Sequence order is reverse of  Power On Condition including Source D-IC.
        4. GCLK On/Off  Sequence
           Normal :  GCLK4 → GCLK5 → GCLK6 → GCLK1 → GCLK2 → GCLK3.
           Reverse :GCLK3 → GCLK2 →GCLK1 → GCLK6 → GCLK5 → GCLK4.
        5. VDD_odd/even  transition time should be within V_ blank
        6. Incase of T6', If there is no  abnormal display, no problem

## 4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at $25\pm2°C$. The values are specified at distance 50cm from the LCD surface at a viewing angle of $\Phi$ and $\theta$ equal to 0 °. FIG. 8 shows additional information concerning the measurement equipment and method.
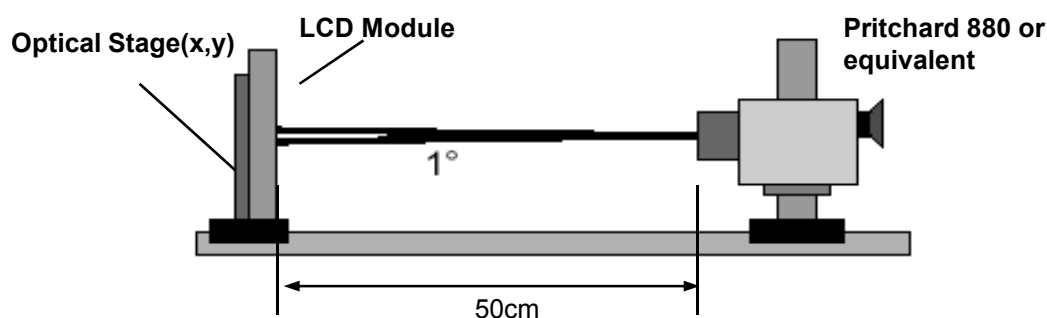


**FIG. 9 Optical Characteristic Measurement Equipment and Method**

Ta= $25\pm2°C$, VDD,H_VDD,VGH,VGL=typ. , fv=120Hz,Clk=297MHz, Vf/If = typ.

**Table 10. OPTICAL CHARACTERISTICS**

| Parameter | | Symbol | | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Contrast Ratio | | CR | | 1100 | 1600 | - | | 1 |
| Surface Luminance, white | | $L_{WH}$ | | 320 | 400 | - | cd/m² | 2 |
| Luminance Variation | | $\delta_{WHITE}$ | 5P | - | - | 1.3 | | 3 |
| Response Time | Rising | Tr | | - | 8 | 12 | ms | **4** |
| | Falling | Tf | | - | 10 | 14 | | |
| Color Coordinates [CIE1931] | RED | Rx | | | 0.644 | | | |
| | | Ry | | | 0.333 | | | |
| | GREEN | Gx | | | 0.306 | | | |
| | | Gy | | Typ -0.03 | 0.604 | Typ +0.03 | | |
| | BLUE | Bx | | | 0.150 | | | |
| | | By | | | 0.058 | | | |
| | WHITE | Wx | | | 0.279 | | | |
| | | Wy | | | 0.292 | | | |
| Color Temperature | | | | | 10,000 | | K | |
| Color Gamut | | | | | 72 | | % | |
| Viewing Angle (CR>10) | | | | | | | | |
| | x axis, right($\phi$=0°) | $\theta r$ | | 89 | - | - | degree | 6 |
| | x axis, left ($\phi$=180°) | $\theta l$ | | 89 | - | - | | |
| | y axis, up ($\phi$=90°) | $\theta u$ | | 89 | - | - | | |
| | y axis, down ($\phi$=270°) | $\theta d$ | | 89 | - | - | | |
| Gray Scale | | | | - | - | - | | 7 |

## Engineering Specification

Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance are determined after the unit has been 'ON' and 1 Hour after lighting the backlight in a dark environment at $25\pm2°C$. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 10.

3. The variation in surface luminance , $\delta$ WHITE is defined as :

$\delta$ WHITE(5P) = Maximum($L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5}$) / Minimum($L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5}$)
Where $L_{on1}$ to $L_{on5}$ are the luminance with all pixels displaying white at 5 locations .
For more information, see the FIG. 10.

4. Response time is the time required for the display to transit from G(255) to G(0) (Rise Time, $Tr_R$) and from G(0) to G(255) (Decay Time, $Tr_D$). For additional information, see the FIG. 11. (N<M)

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 12.

6. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 11.

**Table 11.  GRAY SCALE SPECIFICATION**

| Gray Level | Luminance [%] (Typ) |
|---|---|
| L0 | 0.06 |
| L15 | 0.28 |
| L31 | 1.05 |
| L47 | 2.50 |
| L63 | 4.69 |
| L79 | 7.67 |
| L95 | 11.47 |
| L111 | 16.11 |
| L127 | 21.64 |
| L143 | 28.07 |
| L159 | 35.43 |
| L175 | 43.73 |
| L191 | 52.99 |
| L207 | 63.23 |
| L223 | 74.47 |
| L239 | 86.72 |
| L255 | 100 |

|  | Gray Level | Gamma Ref. |
|---|---|---|
| Positive Voltage | L0 | Gamma9 |
| | L1 | Gamma8 |
| | L31 | Gamma7 |
| | L63 | Gamma6 |
| | L127 | Gamma5 |
| | L191 | Gamma4 |
| | L223 | Gamma3 |
| | L255 | Gamma1 |
| Negative Voltage | L255 | Gamma18 |
| | L223 | Gamma16 |
| | L191 | Gamma15 |
| | L127 | Gamma14 |
| | L63 | Gamma13 |
| | L31 | Gamma12 |
| | L1 | Gamma11 |
| | L0 | Gamma10 |

**Engineering Specification**

Measuring point for surface luminance & measuring point for luminance variation.
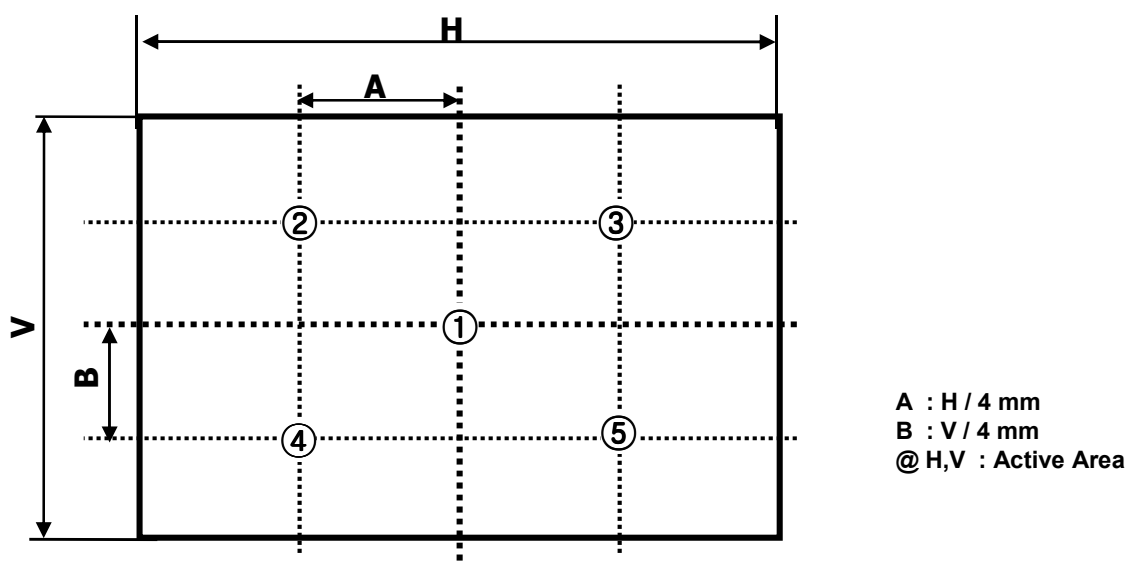


A : H / 4 mm
B : V / 4 mm
@ H,V : Active Area

**FIG. 10  5 Points for Luminance Measure**

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".
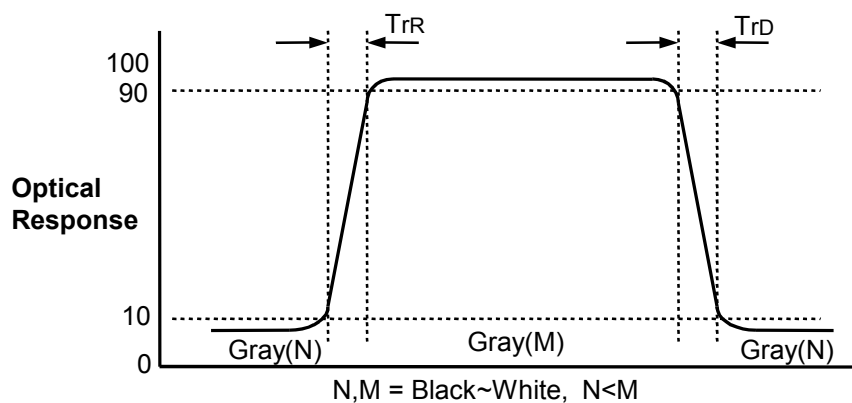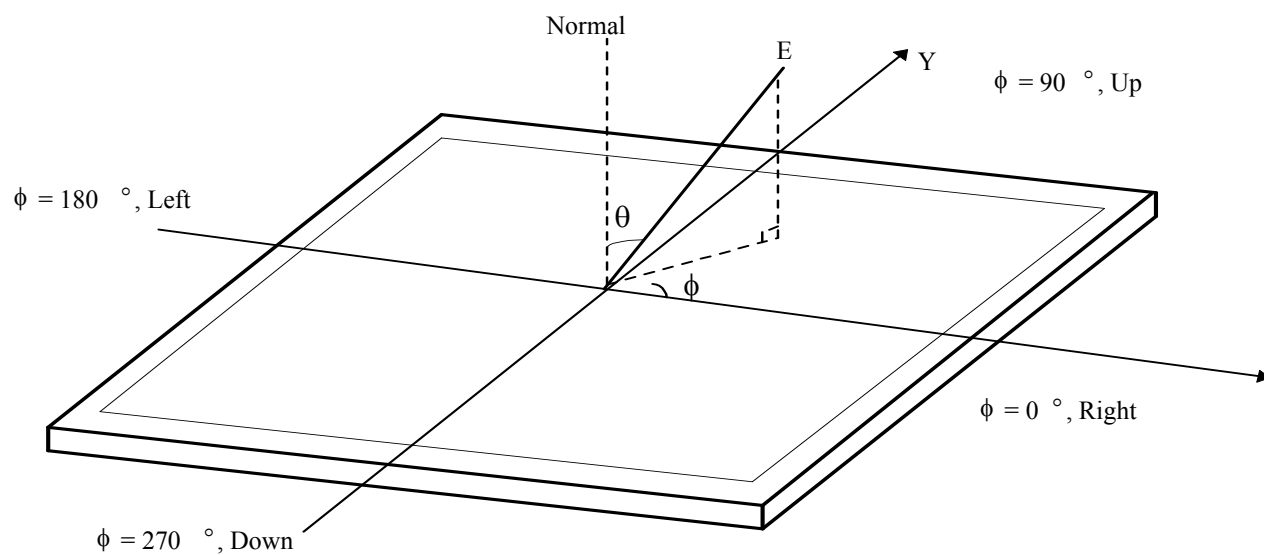


N,M = Black~White,  N<M

**FIG. 11 Response Time**

Dimension of viewing angle range

Normal

E

Y

$\phi = 90$ °, Up

$\phi = 180$ °, Left

$\theta$

$\phi$

$\phi = 0$ °, Right

$\phi = 270$ °, Down

**FIG.12 Viewing Angle**

## 5. Mechanical Characteristics

Table 12 provides general mechanical characteristics.

**Table 12.  MECHANICAL CHARACTERISTICS**

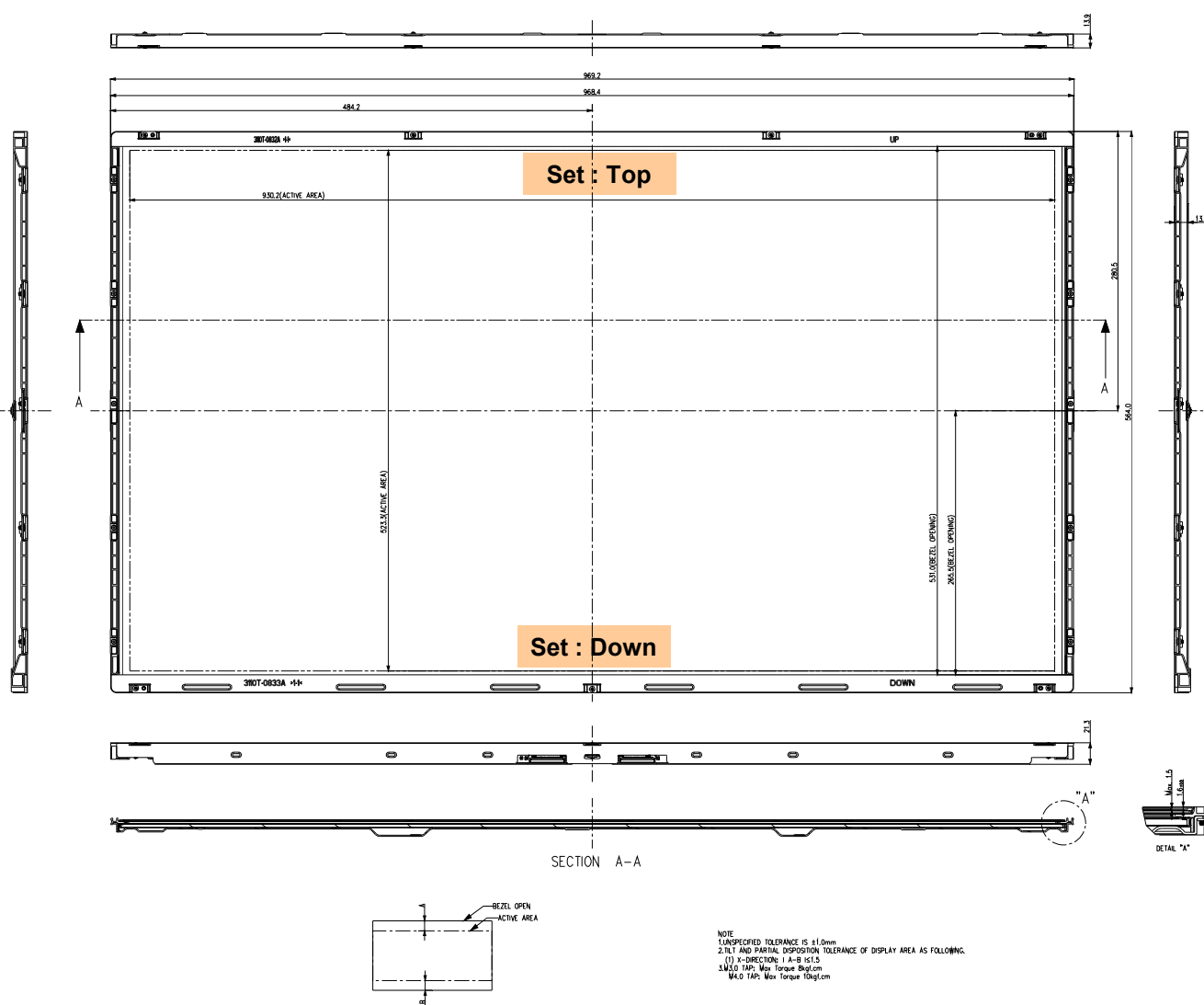| Item | | Value |
|---|---|---|
| Outline Dimension | Horizontal | 968.4 mm |
| | Vertical | 564.0 mm |
| | Depth | 21.3 mm |
| Bezel Area | Horizontal | 944.8 mm (*1) |
| | Vertical | 531.0 mm |
| Active Display Area | Horizontal | 930.24 mm |
| | Vertical | 523.26 mm |
| Weight | 7.0 Kg (Typ.), 7.4 kg (Max.) | |

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.
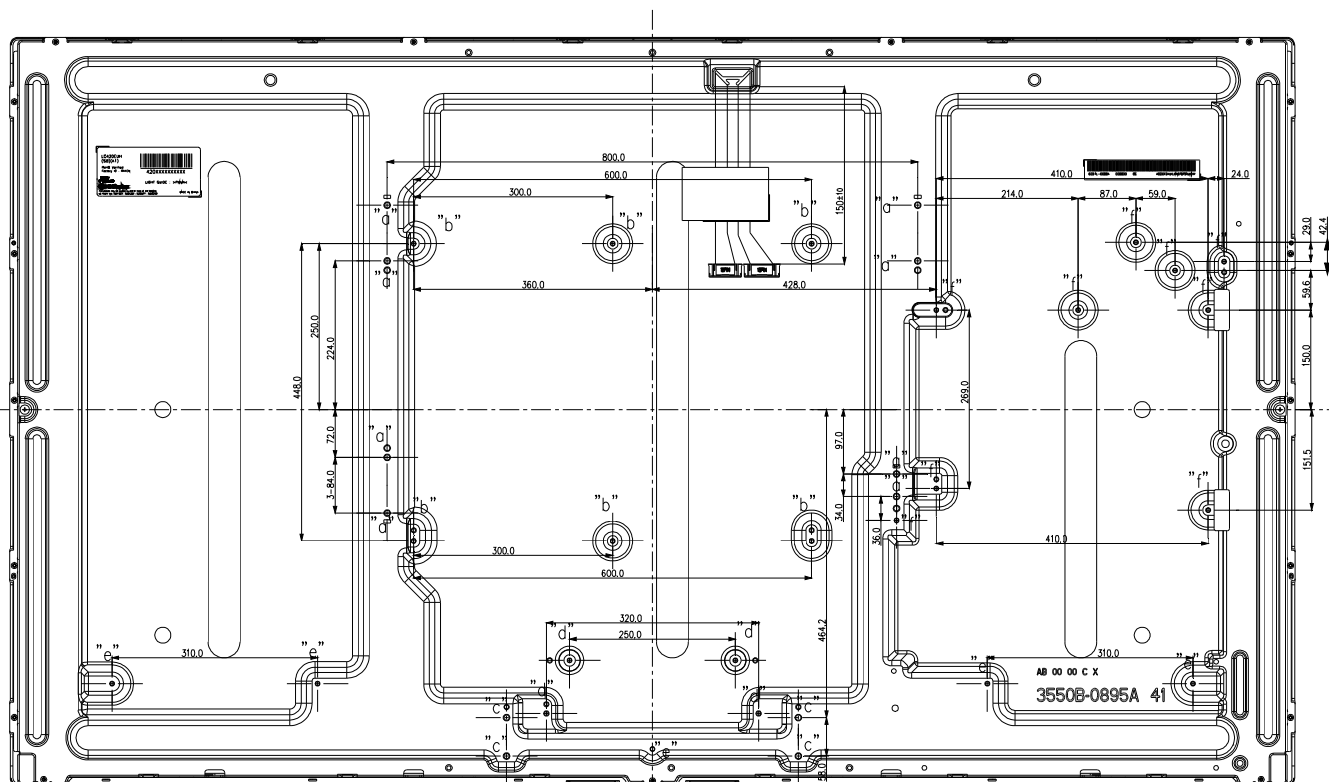*1: The horizontal dimension of bezel area is based on polarizer.

## Engineering Specification

**[ FRONT VIEW ]**



SECTION A-A

BEZEL OPEN
ACTIVE AREA

NOTE
1.UNSPECIFIED TOLERANCE IS ±1.0mm
2.TILT AND PARTIAL DISPOSITION TOLERANCE OF DISPLAY AREA AS FOLLOWING.
   (1) X-DIRECTION; I A-B I≤1.5
3.M3.0 TAP; Max Torque 8kgf.cm
   M4.0 TAP; Max Torque 10kgf.cm

**Engineering Specification**

**[ REAR VIEW ]**



<TAP INFORMATION>

| ITEM | TAP | MAX DEPTH(mm) | TORQUE(Kgf.cm) | NOTES |
|------|-----|---------------|----------------|-------|
| "a" | M4 | 7.5 | Max. 10.0 | – |
| "b" | M3 | 8.0 | Max. 8.0 | – |
| "c" | M4 | 7.5 | Max. 10.0 | – |
| "d" | M3 | 4.5 | Max. 8.0 | – |
| "e" | M3 | 7.5 | Max. 8.0 | – |
| "f" | M3 | 8.0 | Max. 8.0 | – |

Engineering Specification

# 6. Reliability

**Table 13.  ENVIRONMENT TEST CONDITION**

| No. | Test Item | Condition |
|-----|-----------|-----------|
| 1 | High temperature storage test | Ta= 60°C   240h |
| 2 | Low temperature storage test | Ta= -20°C  240h |
| 3 | High temperature operation test | Ta= 50°C   50%RH    240h |
| 4 | Low temperature operation test | Ta= 0°C    240h |
| 5 | Humidity condition Operation | Ta= 40 °C ,90%RH |

Note :  Before and after Reliability test,  LCM should be operated with normal function.

## 7. International Standards

## 7-1. LED Array - Safty

1. Laser (LED Backlight) Information

```
Class 1M LED Product
IEC60825-1 : 2001
Embedded LED Power (Class 1M)
```

2. Caution
   : LED inside.
     Class 1M laser (LEDs) radiation when open.
     Do not  open while operating.

## 7-2. Environment

   a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

| Engineering Specification |
| :-: |

## 8. Precautions

Please pay attention to the followings when you use this TFT LCD module.

## 8-1. Mounting Precautions

(1) You must mount a module using specified mounting holes (Details refer to the drawings).
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
   Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

## 8-2. Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
   V=$\pm$200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
   And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer
(4) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
(8) A screw which is fastened up the steels should be a machine screw.
   (if not, it can causes conductive particles and deal LCM a fatal blow)
(9) Please do not set LCD on its edge.
(10) The conductive material and signal cables are kept away from LED driver inductor to prevent abnormal display, sound noise and temperature rising.

## 8-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

## 8-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

## 8-5. Storage

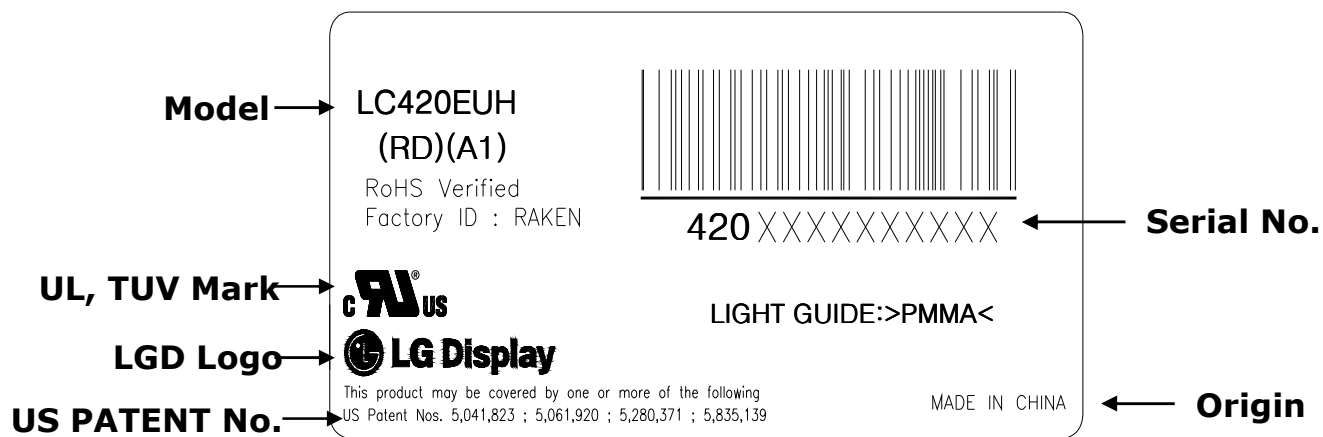When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.
(3) Storage condition is guaranteed under packing conditions.
(4) The phase transition of Liquid Crystal could be recovered if the LCM is released at the normal condition after the low or over the storage temperature.

## 8-6. Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a  very small amount of glue still on the bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is  recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.
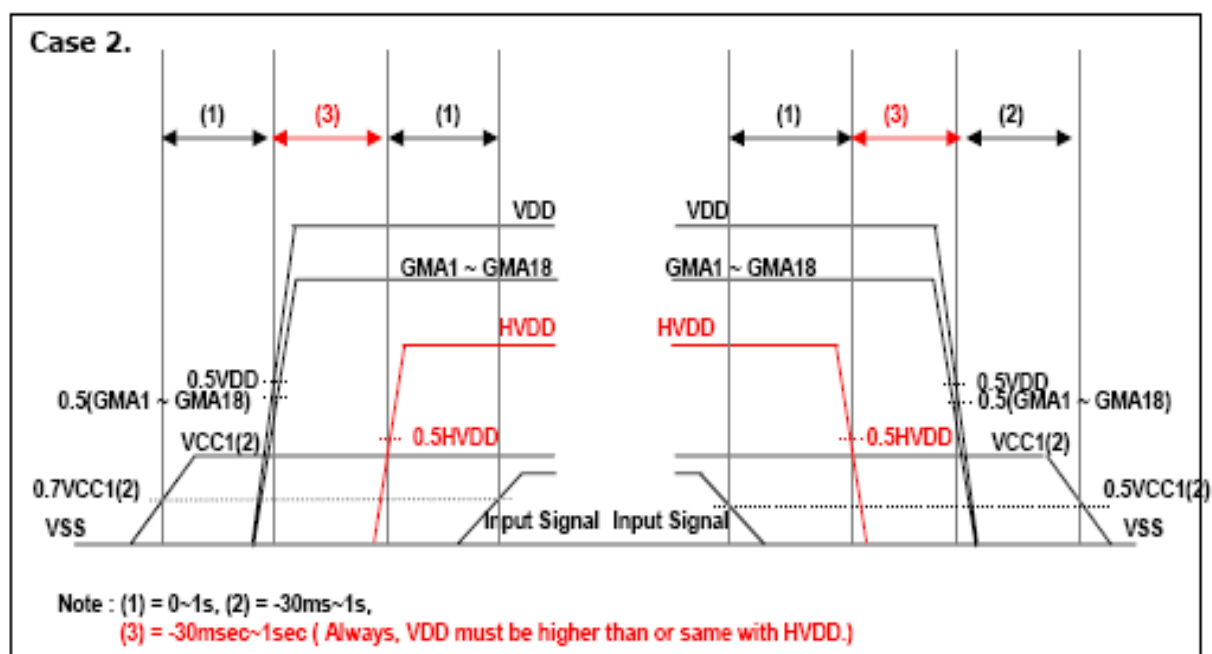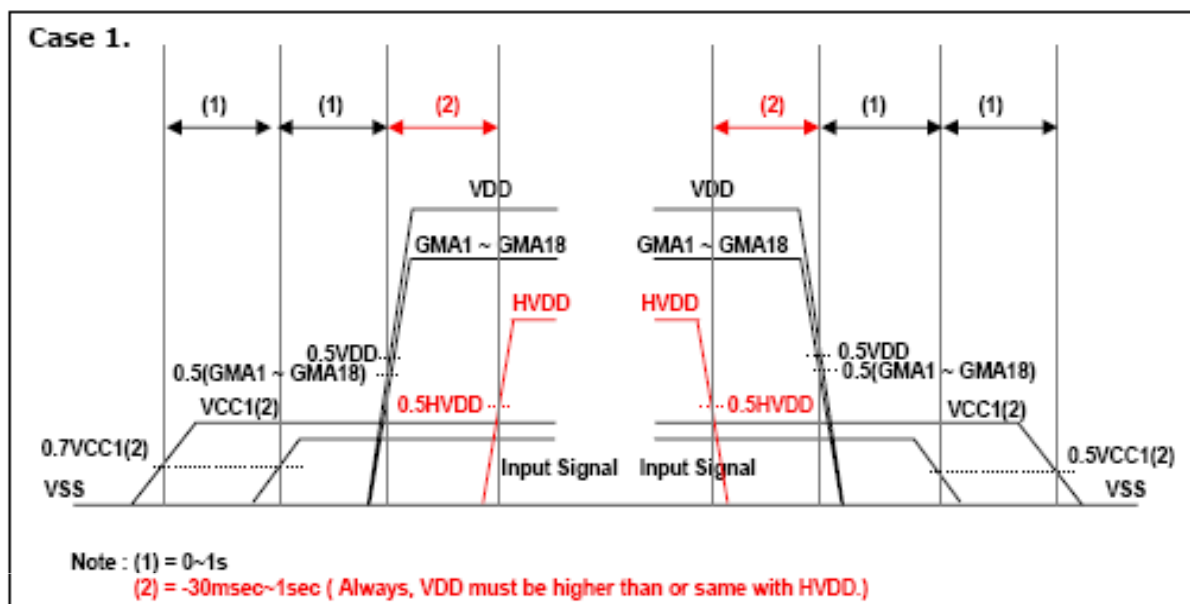
# # APPENDIX- I
■ LCM Label

Model → LC420EUH
(RD)(A1)
RoHS Verified
Factory ID : RAKEN

420 XXXXXXXXXX ← Serial No.

LIGHT GUIDE:>PMMA<

UL, TUV Mark →

LGD Logo → LG Display

US PATENT No. → This product may be covered by one or more of the following
US Patent Nos. 5,041,823 ; 5,061,920 ; 5,280,371 ; 5,835,139

MADE IN CHINA ← Origin

# APPENDIX-11

■ LCM Source power sequence

**< Source power sequence >**



Case 1.

Note : (1) = 0~1s
(2) = -30msec~1sec ( Always, VDD must be higher than or same with HVDD.)

Case 2.

Note : (1) = 0~1s, (2) = -30ms~1s,
(3) = -30msec~1sec ( Always, VDD must be higher than or same with HVDD.)

**- Input Signal : SOE,POL,GSP,H_CONV,OPT_N**

**RAKEN**

Engineering Specification

# # APPENDIX- III

## ■ LED Array Electrical Spec

| Items | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Array Operating Voltage | $V_F$ | $I_{FM}$=800mA *1) | 40.6 | 44 | 47.6 | V |
| | $\triangle Vop$ *2) | $I_{FM}$=800mA | - | - | 1.7 | V |

※ Typ. IF=800[mA] *1) : This value is determined by the specific LED current ( 100mA per LED )
※ $\triangle Vf$ *2) of each string is 1.7V at max. in 1 BLU set without driver, however the $\triangle Vf$ of BLU set
with driver could be allowed to 1.7V at max. in single array
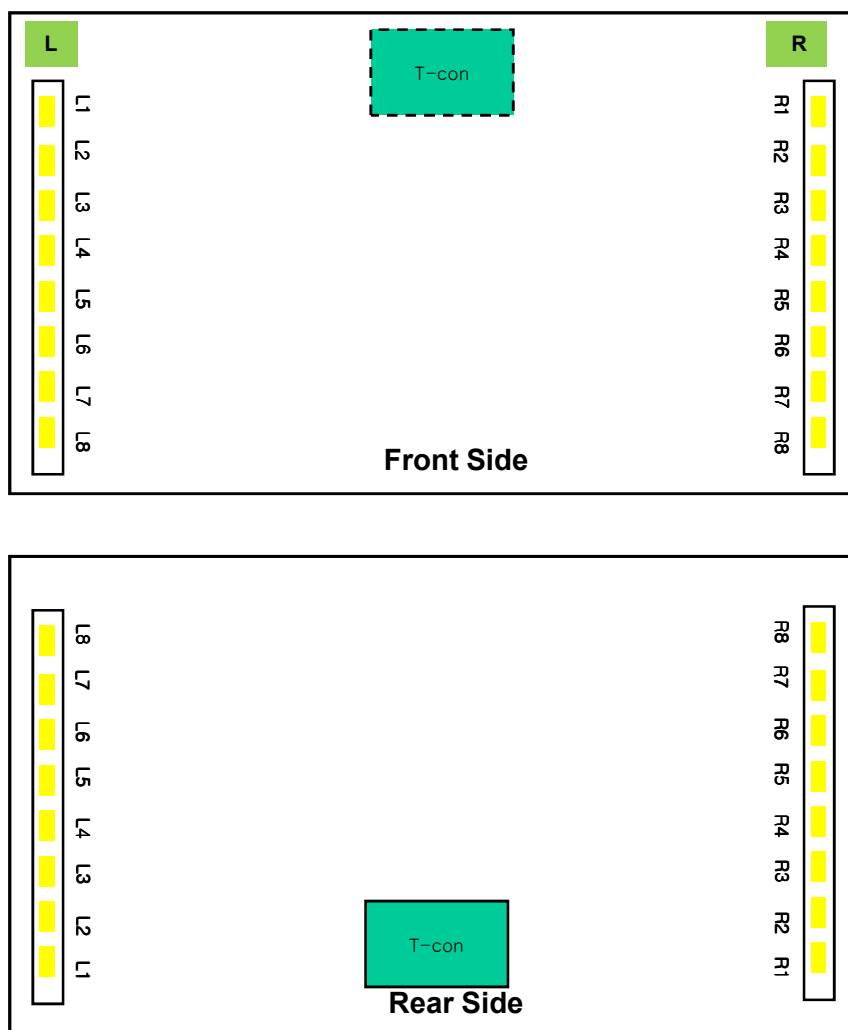
## ■ Forward Current vs. Forward Voltage
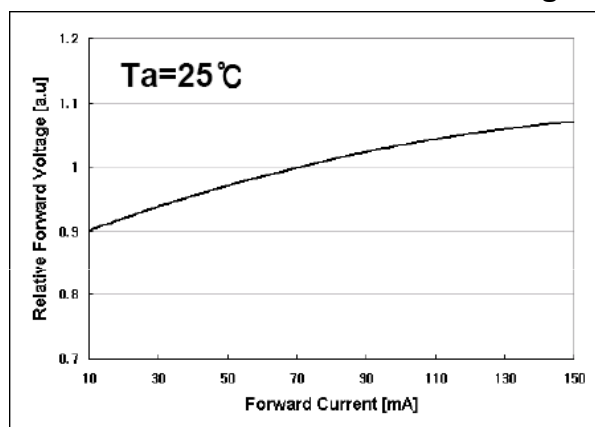


## ■ Ambient Temperature vs. Forward Voltage
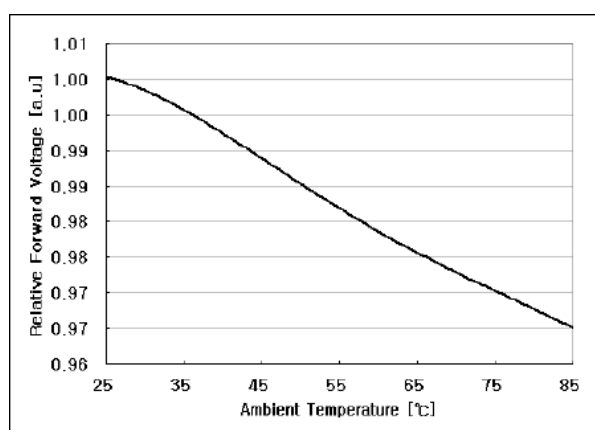
# # APPENDIX- IV

## ■ Local Dimming Block Pin Matching



**Front Side**



**Rear Side**

| LED Driver CNT | | |
|---|---|---|
| **Pin No** | **CN_201** | **CN_202** |
| 1 | Anode_L1 (1~4Cathode) | Anode_R2 (5~8Cathode) |
| 2 | N.C | N.C |
| 3 | L1 Cathode | R8Cathode |
| 4 | L2 Cathode | R7 Cathode |
| 5 | L3 Cathode | R6 Cathode |
| 6 | L4 Cathode | R5 Cathode |
| 7 | N.C | R4 Cathode |
| 8 | L5 Cathode | R3 Cathode |
| 9 | L6 Cathode | R2 Cathode |
| 10 | L7 Cathode | R1 Cathode |
| 11 | L8 Cathode | N.C |
| 12 | N.C | Anode_R1 (1~4Cathode) |
| 13 | Anode_L2 (5~8Cathode) | - |